Towards Photonic Integrated Circuits; Design and Fabrication of Passive InP Waveguide Bends

by

Sarah Rodriguez

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Author ....
Sarah Rodriguez
Department of Electrical Engineering and Computer Science
May 7, 2004

Certified by ....
Leslie A. Kolodziejski
Professor of Electrical Engineering and Computer Science
Thesis Supervisor

Accepted by ....
Arthur C. Smith
Chairman, Department Committee for Graduate Students

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ABSTRACT

Waveguide bends, fabricated in the (In,Ga)(As,P) material system, have been simulated, fabricated and tested. A process is developed for waveguides of 1 μm through 7 μm widths. Waveguides containing S-bends of varying bending radii as well as resonator bends were examined. RESULTS TBD

Thesis Supervisor: Leslie A. Kolodziejski
Professor of Electrical Engineering and Computer Science

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1.0 INTRODUCTION

Efforts for improving communication systems have been made for centuries, starting with written communication systems to modern optical network systems. There is a constant need for making networks with lower loss, higher speed and low cost. Photonic integrated circuits (PIC) provide an efficient way for meeting these demands. PICs will eliminate the need for separate components in the network and perform all of the necessary functions on a single chip, such as amplification, switching, transmitting and receiving to name a few.

Photonic integrated circuits provide an valuable integrated technology platform for use in optical communications. PICs may consist of a number of devices, such as layers and isolaters to name a few, integrated with the use of waveguides.

FIGURE 1.1 Unit optical logic cell

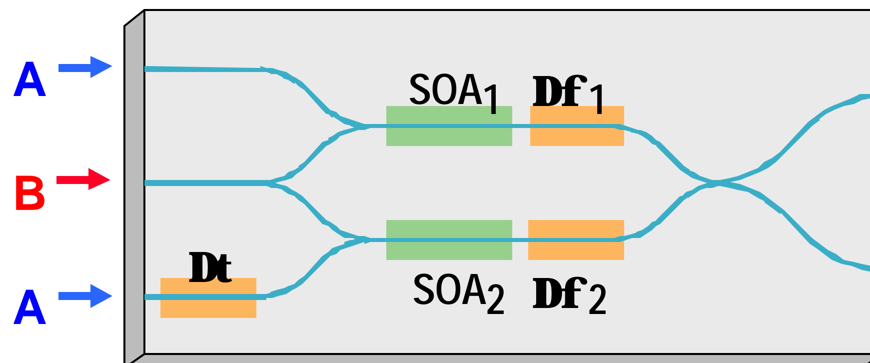


Figure 1.1 depicts an optical logic cell with the blue lines representing the waveguides. One of the major design issues associated with waveguides is the amount of space required for waveguide bends. While tighter bends require less space, they are more prone to radiation loss. In order to reduce the overall size of future PIC devices, a compact low loss solution to waveguide bending must be found.

This thesis will focus on low loss waveguide bending. Waveguide bends will be Simulated, designed, fabricated and tested. Chapter two will conation an overview of the theory behind dielectric waveguides, a survey of past research on the topic, simulated results and the design of the waveguide bends. Chapter three contains a brief overview of the fabrication process while, chapter four contains the processes in more detail with results. Measurement procedures and the experi-

mental data of the fabricated waveguides are discussed in chapter five. A summary and conlcusion of this work is contained in chapter six.

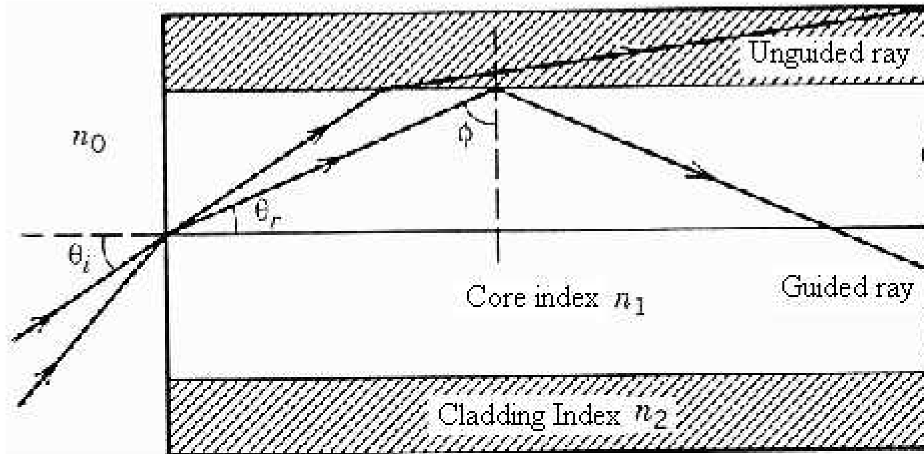
2.0 DESIGN THEORY & SIMULATION

2.1 Waveguide Theory

2.1.1 Total Internal Reflection

There are many considerations which must be taken into account while designing waveguides. One concept of importance is total internal reflection. Figure 2.2 depicts the concept of total internal reflection through the use of a ray diagram of an optical fiber.

FIGURE 2.2 Light confinement through total internal reflection in a step-index fiber [1]



As the diagram shows, the unguided ray is transmitted through the core index into the cladding index. The guided ray is completely reflected throughout the fiber, remaining in the core index. It would be ideal to have information travel in optical waveguides through guided rays, greatly reducing loss.

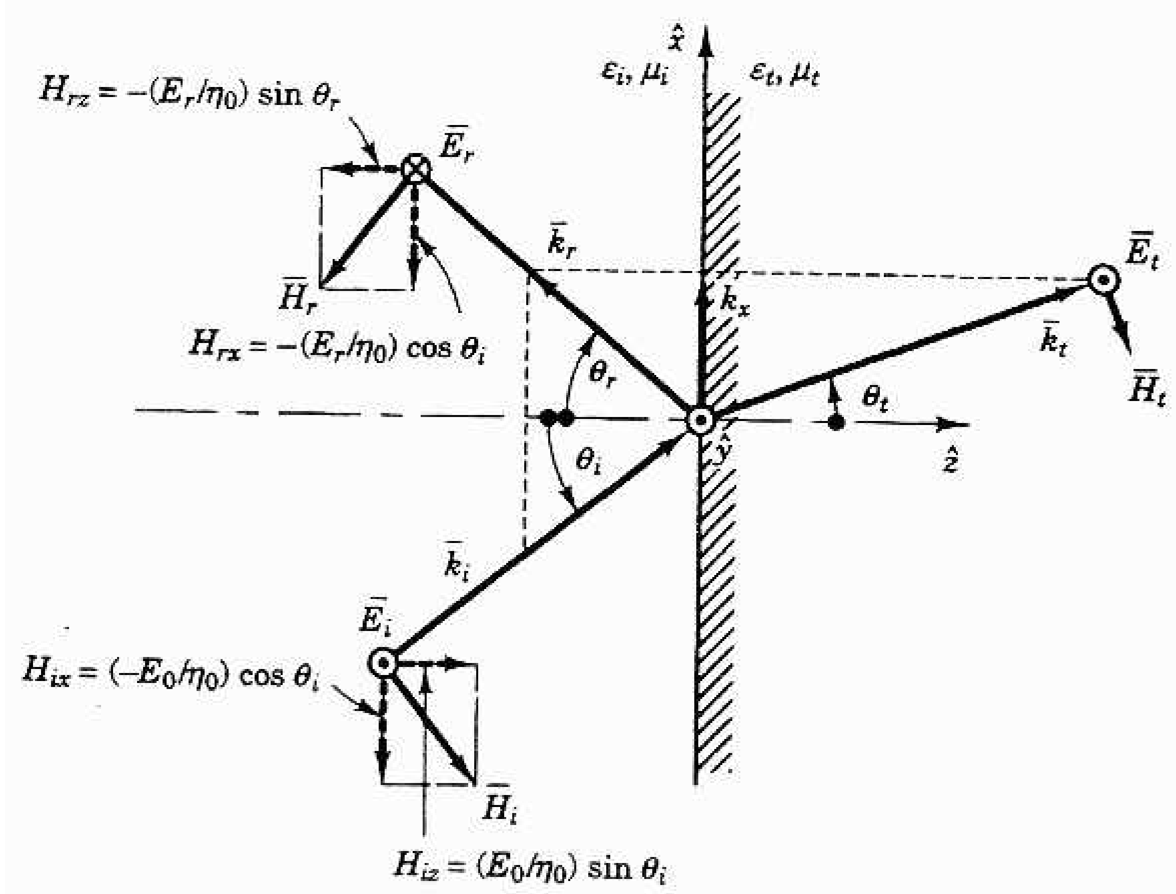
In order to get a better understanding for how total internal refection takes place, attention is focused on plane waves incident upon a planar boundary. Figure 2.3 illustrates a transverse electric (TE) wave incident at an angle θ upon a boundary. **k** represents the propagation vector of the traveling wave. The subscripts i, r and t represent the incident, reflected and transmitted components of the wave respectively. For simplicity, the place of incidence is defined in the x-z plane. Upon inspection of the diagram, the propagation vector may be written as follows:

$$\bar{k}_i = \hat{x}k_{ix} + \hat{z}k_{iz} \quad \text{(EQ 2.1)}$$

$$\bar{k}_r = \hat{x}k_{rx} - \hat{z}k_{rz} \quad \text{(EQ 2.2)}$$

$$\bar{k}_t = \hat{x}k_{tx} + \hat{z}k_{tz} \quad \text{(EQ 2.3)}$$

FIGURE 2.3 TE wave incident upon a planar boundary [2]



The phase matching condition states the tangential components of the electric and magnetic fields must be continuous for all x and time. Therefore, the tangential components for all three k vectors must be equal along the boundary, leading to equation [2.4].

$$k_x = k_i \sin\theta i = k_r \sin\theta r = k_t \sin\theta t \quad \text{(EQ 2.4)}$$

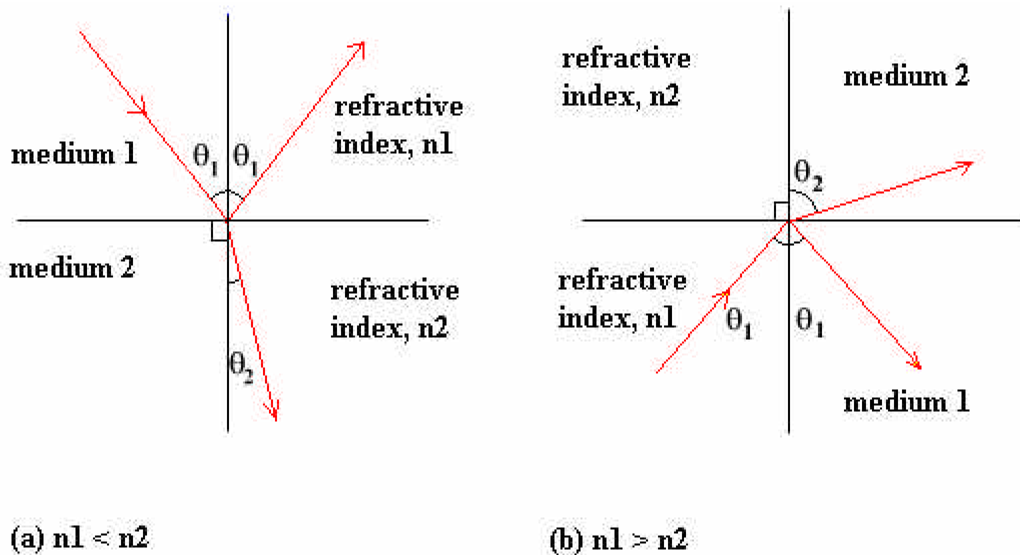
Since the reflected and incident wave travel in the same medium, they have the same dispersion relation, therefore the magnitudes of their propagation vectors are equal. From equation 2.4, since the magnitudes of the propagation vectors are

equal, the incident and reflected angles are also equal, which leads to the following equation:

$$\frac{\sin\theta t}{\sin\theta i} = \frac{n_i}{n_t} \quad \text{(EQ 2.5)}$$

Equation 2.5 is commonly referred to as Snell's law. Snell's law demonstrates how the relation between the angle of transmission and reflection are dependent on the indices of refraction of both the incident and transmitted medium. Figure 2.4 portrays a pictorial description of Snell's Law.

FIGURE 2.4 (a) Illustrates the case where the transmitting medium has a higher refractive index than the medium in which the incident wave travels. (b) Illustrates the case where the transmitting medium has a lower refractive index than the medium in which the incident wave travels [3]



In Figure 2.4 (a), an incident wave traveles from a lower index of refraction to a higher index of refraction. Figure 2.4 (b) portrays the opposite case of an incident wave traveling from a higher index of refraction to a lower index of refraction. As seen from the diagram, a light ray traveling from an index of higher refraction to an index of lower refraction, will bend further away from the normal of the boundary surface.

In the case of Figure 2.4 (b), if the value of θ_1 were to be increased, there would be a certain value, θ_c where total internal reflection would take place. θ_c is commonly known as the critical angle. When the incident angle equals the critical

angle, the transmitted angle equals 90°, therefore the light propagates parallel to the boundary surface. In the case of $\theta_1 = \theta_c$, Snell's law gives us the following result:

$$\frac{\sin\theta_t}{\sin\theta_c} = \frac{1}{\sin\theta_c} = \frac{n_i}{n_t} \quad \textbf{(EQ 2.6)}$$

$$\theta_c = \operatorname{asin}\left(\frac{n_t}{n_i}\right) \quad \textbf{(EQ 2.7)}$$

For θ_1 values larger than θ_c, the transmitted wave exponentially decreases from the boundary surface, this is called an evanescent wave. Since no average power is transmitted into the second medium, in the case of evanescent waves, total internal reflection is achieved.

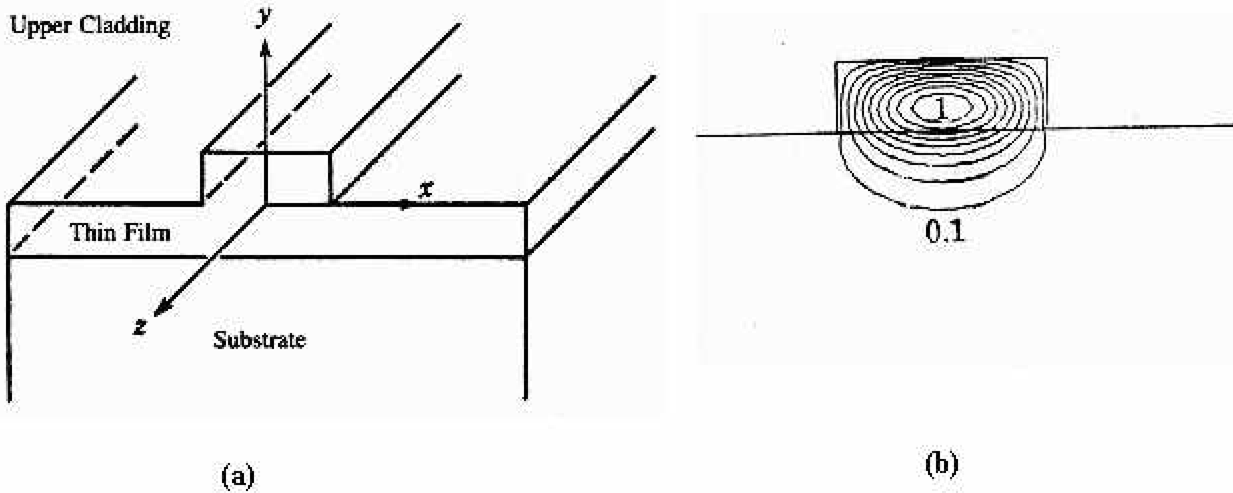
Using equation [2.5] and equation [2.6], one can find the maximum allowed angle for the total internal reflection condition.

$$\theta_{max} = n_1 \cos\theta_c = (n_1^{\,2} - n_2^{\,2})^{\frac{1}{2}} \quad \textbf{(EQ 2.8)}$$

2.1.2 Dielectric Waveguides

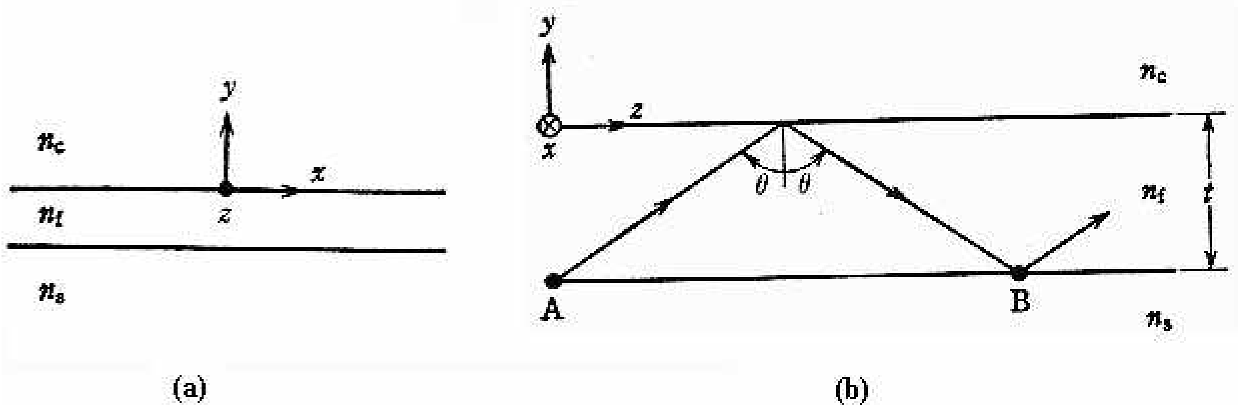
By inserting a layer of material which contains a higher refractive index than the substrate and the upper cladding, on the substrate surface, light can be trapped inside the film by total internal reflection. A rectangular dielectric waveguide will trap light in both the horizontal and vertical directions, providing modal confinement. Figure 2.5 provides a pictorial example of a rectangular dielectric waveguide and a simulated mode profile.

FIGURE 2.5 Example of a dielectric waveguide (a). Simulated mode profile (b) [4]



In multi-layered dielectric waveguides, special attention must be given to the effective index of refraction of the guiding layer. The front and side view of a three layer dielectric waveguide are portrayed in Figure 2.6 (a) and (b) respectively.

FIGURE 2.6 Front (a) and side (b) view of a three layer dielectric waveguide [4]



In order for the condition of total internal reflection to be met, the effective index of refraction must be greater than the index of the cladding and substrate. For a

plane wave incident on the dielectric waveguide in Figure 2.6 (b), its phase constant β is given by:

$$\beta = k_o n_f \sin\theta \quad \text{(EQ 2.9)}$$

Where the effective index, n_{eff}, is given by:

$$n_{eff} \equiv \frac{\beta}{k_o} = n_f \sin\theta \quad \text{(EQ 2.10)}$$

The critical angles at the guiding layer substrate surface and the guiding layer cladding surface, can be dervied using equation [2.7]:

$$\theta_{substrate} = \operatorname{asin}\left(\frac{n_s}{n_f}\right) \quad \text{(EQ 2.11)}$$

$$\theta_{cladding} = \operatorname{asin}\left(\frac{n_c}{n_f}\right) \quad \text{(EQ 2.12)}$$

In order for the total internal reflection condition to be met, n_c < or = $n_s < n_f$ must be satisfied, therefore the effective index of the guiding layer must be greater than that of the substrate and cladding layers.

2.2 Survey of Past Work

2.2.1 Waveguide Bend Fabrication

A significant effort has been put forth in the design of waveguide bends, a number of researchers have examined methods for creating low loss waveguide bends. M. Austin has fabricated rib waveguides on GaAs/$Ga_{0.82}Al_{0.18}As$ and GaAs/$Ga_{0.92}Al_{0.08}As$ slices grown by MO-CVD [5]. The waveguides were 3µm wide and contained 90° bends with 75, 100, 125, 125, 150, 200, 250, 300, and 400 µm radii.

Austin discovered that minimizing the bending loss while reducing the radius of curvature, could be achieved by creating waveguides with large rib heights. The larger rib heights, predominately surrounded by air, increased lateral confinement. Reducing the height of the slab adjacent to the rib structure was also found to increase the lateral confinement as well as reduce the number of allowable modes. Insertion losses were also found to be smaller for guides with larger rib heights.

Austin showed that in his case, a minimum loss (approximately 3 dB) for multimode guides bending at 90° occured when a radius of curvature was 300µm. An

8.5 dB minimum loss was achieved for a single-mode curved guide with a radius of curvature of 400 μm. Austin noted more work was needed with guides of different geometries, material composition and waveguides thicknesses to determine the limiting loss mechanisms.

2.2.2 Waveguide Bend & Offset Simulation

Rajarajan, et al, made use of various numerical methods along with variations of waveguide parameters to simulate waveguide bends [6]. Offsets were used as a means of reducing the loss. In a curved waveguide, the mode profile shifts to the outer edge of the bend which causes a field mismatch at the junction between a straight and bend waveguide. An offset will improve the coupling between the straight and bent sections of the waveguide.

A vectorial finite element-based beam propagation method was used to find the radiation losses and the changes in the mode profile along the waveguide bends. A least squares boundary residual method (LSBR) is used to find the transmission and reflection coefficients at the straight-to-bent waveguide junctions and for offset optimizations. The initial waveguide, that was used for the numerical simulations, consisted of a GaAs guiding layer placed on a thick 7μm layer of $Al_{0.15}Ga_{0.85}As$. The height and width of the rib were 0.4μm and 3μm respectively. The waveguides also contain an epilayer, a layer abour the substrate and below the rib structure, of 0.4μm. At the simulation wavelength of 1.15μm, the refractive indices of the GaAs and AlGaAs are 3.44 and 33.5 respectively. The waveguides contained 90° bends with a radius of 100μm.

The simulations with the initial parameters showed a loss of 16 dB/90°. A minimum loss value was found to be 1dB/90° for a waveguide with a radius of 275μm. Although the increase in bending radius greatly reduced the loss, tighter bends are much more desired. It was found that reducing the epilayer thickness resulted in the center of the optical mode moving further upwards, radiating less to the outer slab layer, therefore decreasing the loss. Decreasing the epilayer from 0.4μm to 0.3μm lead to a reduced loss of 10 dB/90°. It was noted that completely removing the epilayer would enable the design of low loss compact waveguide bends. For radii of 150μm and 200μm, the bending loss was found to be a minimum with a rib width of 1.9μm. The waveguide became multimode when the rib width was increased beyond 1.85μm. Initial simulations showed the center of the mode profile shifted to the right by more than 1μm after the bend. The transition loss with the initial parameters was found to be 6.5 dB. An offset of 1.3μm provided a minimum transition loss of 2.2 dB. Introducing offsets not only reduced the transition loss but also reduced the reflection coefficient as well. The required offset for both TE and TM polarizations were found to be almost identical down to a bending

radius of 400µm. For radii smaller than 400µm, the required offsets increased linearly.

Seo, et al, have also investigated losses in waveguide bends with the use of numerical simulations [7]. In addition to offsets, the researchers used isolation trenches next to the waveguide structure as means of reducing transition losses. Placing a trench outside the curved waveguide prevents light from spreading outward toward larger radii, thus improving beam confinement.

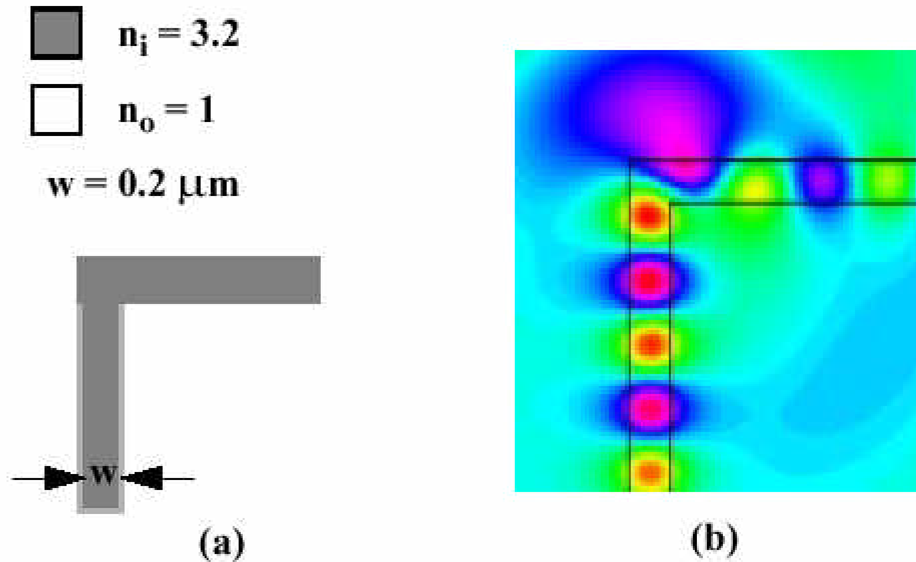
A 3-D semivectorial finite difference beam propagation program was used for the simulations. Simulations provided the following optimal values; rib height and width of 1.4µm and 2.4µm respectively, offset of 0.5µm, trench distance and width of 2µm and 4µm respectively and an epilayer thickness of 0.4µm. The simulations were calculated on a GaAs/GaAlAs sturcture with a bending radius of 1.5mm and a wavelength of 1.5µm.

All the optimizations were calculated with a rib height of 1.4µm, although it was noted a further reduction of transition loss could be achieved by increasing the height of the rib. Higher rib heights increase the effective index of the rib so that more light is confined by the rib. Simulations found an asymmetric mode in the curved waveguide section and a symmetric mode in the straight waveguide section. A solution to the modal symmetry program was found by sloping the rib walls. The authors proposed having different slopes for the right and left side walls for the rib, stating that the asymmetry in the rib will counter the asymmetry in the bend. It was noted that fabrication of such a configuration would be hard to obtain, placing the sample at an angle during the etching process was suggested.

2.2.3 Total Internal Reflection Bend

C. Manolatou et al [8] used the concept and design of total internal reflection to design compact waveguide bends. Manolatou et al discovered the performance of sharp 90° bends in high contrast, single mode waveguides could be enhanced with the placement of a resonant cavity at the corner of the guide. The radiation loss due to the mode mismatch at the corner of the bends, were reduced by achieving strong coupling of the waveguide modes to the resonator modes. Figure 2.7 shows the simulated electric field amplitude results of transmission through a sharp 90° bend, a great amount of radiation loss was incurred as light transversed through the bend.

FIGURE 2.7 (a) Drawing of a sharp 90° bend. (b) Electric field amplitude in the bend.[8]



A first attempt of placing a resonant cavity at the corner of teh guide, was done by increasing the volume of the dielectric at the corner region to form a square resonator. Figure 2.8 displays the simulated results. The electric field pattern shows a great reduction of the radiation loss but poor transmission was detected and reported with the use of other simulation programs. In order to further improve the bend, the coupling between the cavity and the waveguide mode relative to the coupling radiation, was increased. This was achieved by pushing the cavity mode at the corner region inwards in order to obtain better mode matching. The waveguide bend, shown in Figure 2.9, depicts a waveguide with these further improvements, in which a cut on the corner of the waveguide was used to produced the desired effects. The final improvemed total internal reflection bends almost completely eliminate the radiation loss while containing a transmission of nearly 99%, as was reported with use of simulation programs.

FIGURE 2.8 (a) Drawing and (b) electric field amplitude of improvement bend. [8]

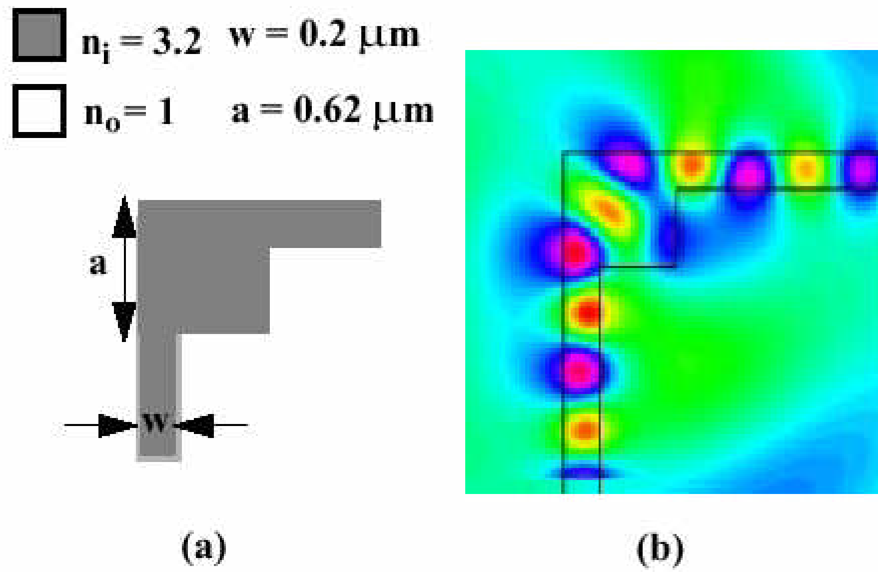
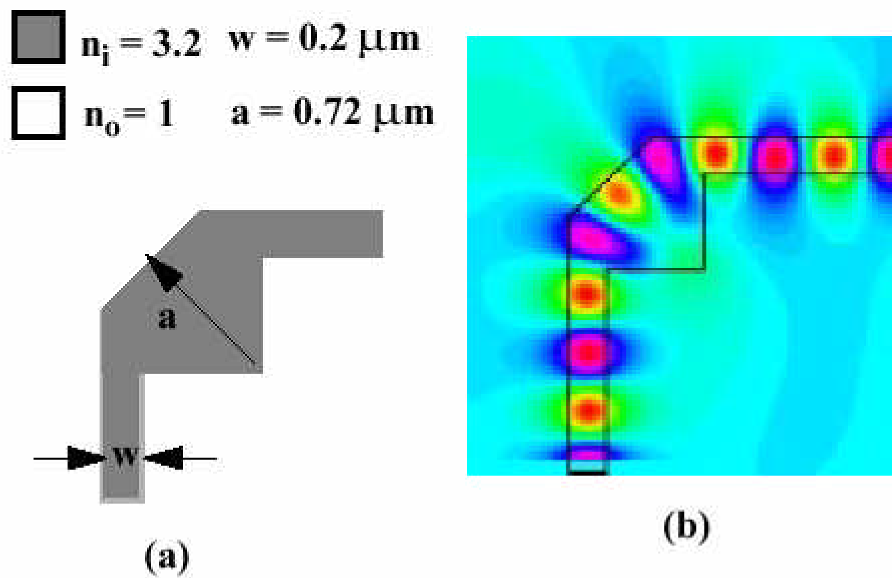


FIGURE 2.9 (a) Drawing and (b) electric field amplitude of the final improvement bend. [8]



2.3 Design & Simulations

2.3.1 Straight Waveguide Simulation

The goal is to fabricate and test waveguide bends in the (In,Ga)(As,P) material system. For use in photonic integrated circuits, $In_{1-x}Ga_xAs_yP_{1-y}$ lattice matched to InP, offers a bandgap range which is compatible with optical fiber networks. In order to achieve a single mode waveguide with good mode confinement, the effective index of the passive waveguide should be above InP (n=3.167) but well below that of the active material (n=3.424). A waveguide with a low effective index may be obtained by alternating a quarternary layer ($In_{0.56}Ga_{0.44}As_{0.95}P_{0.07}$, n=3.294) with InP layers. Two different structures have been grown; R998 and R1007. The grown structures differ in the thicknesses for the quaternary and InP layers. The mode profile simulations have been preformed on Rsoft, a beam propagation simulation program. Both R998 and R1007 were simulated for mode profiles with widths ranging from 1µm to 7µm and a fixed height of 1.2µm. Figure 2.10 through Figure 2.23 are the simulated results for the various straight waveguides, where Z is the length along the waveguide where the mode profile has been calculated.

FIGURE 2.10 (a) Waveguide design R998 width = 1µm and (b) associated mode profile (Z=48)

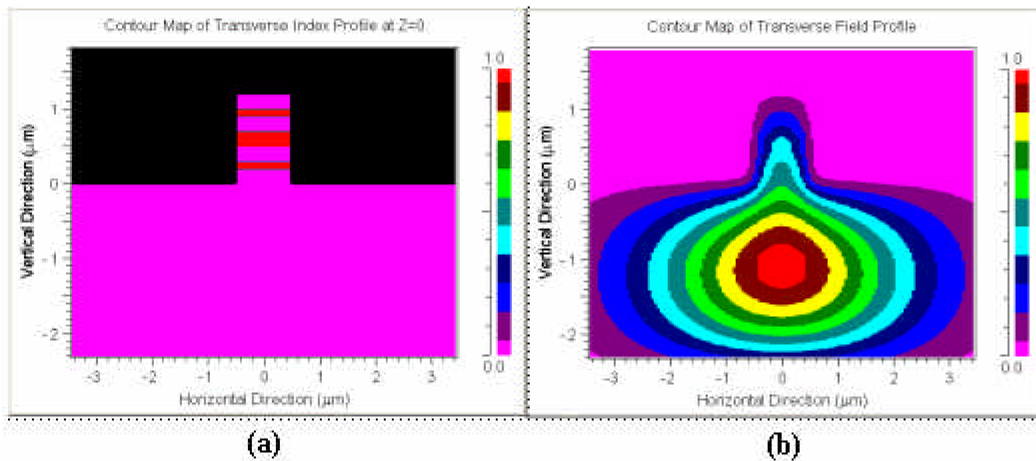


FIGURE 2.11 (a) Waveguide design R998 width = 2µm and (b) associated mode profile (Z=240)

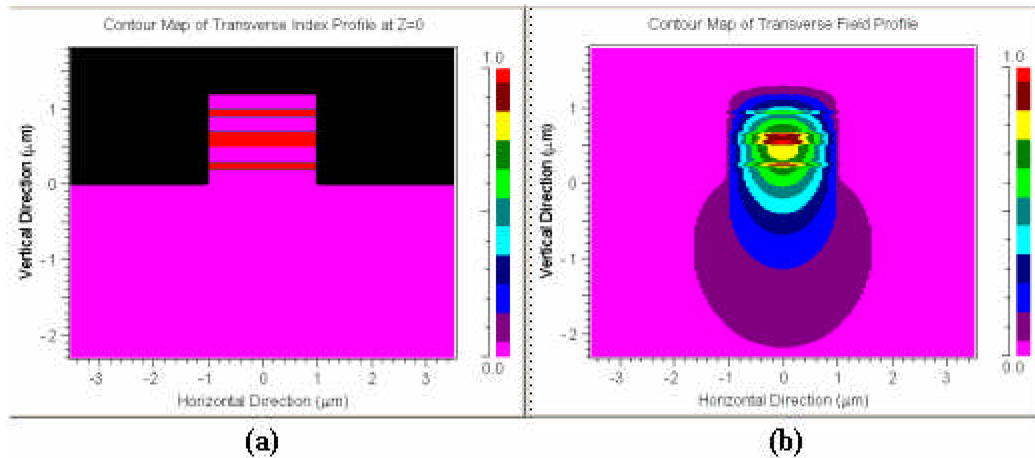


FIGURE 2.12 (a) Waveguide design R998 width = 3µm and (b) associated mode profile (Z=108)

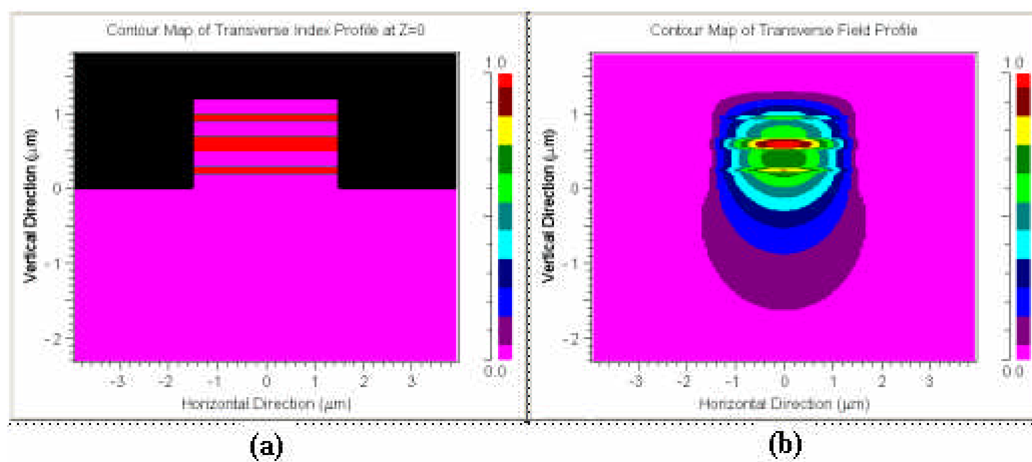


FIGURE 2.13 (a) Waveguide design R998 width = 4µm, (b) associated mode profile (Z=20) and (c) associated mode profile (Z=400)

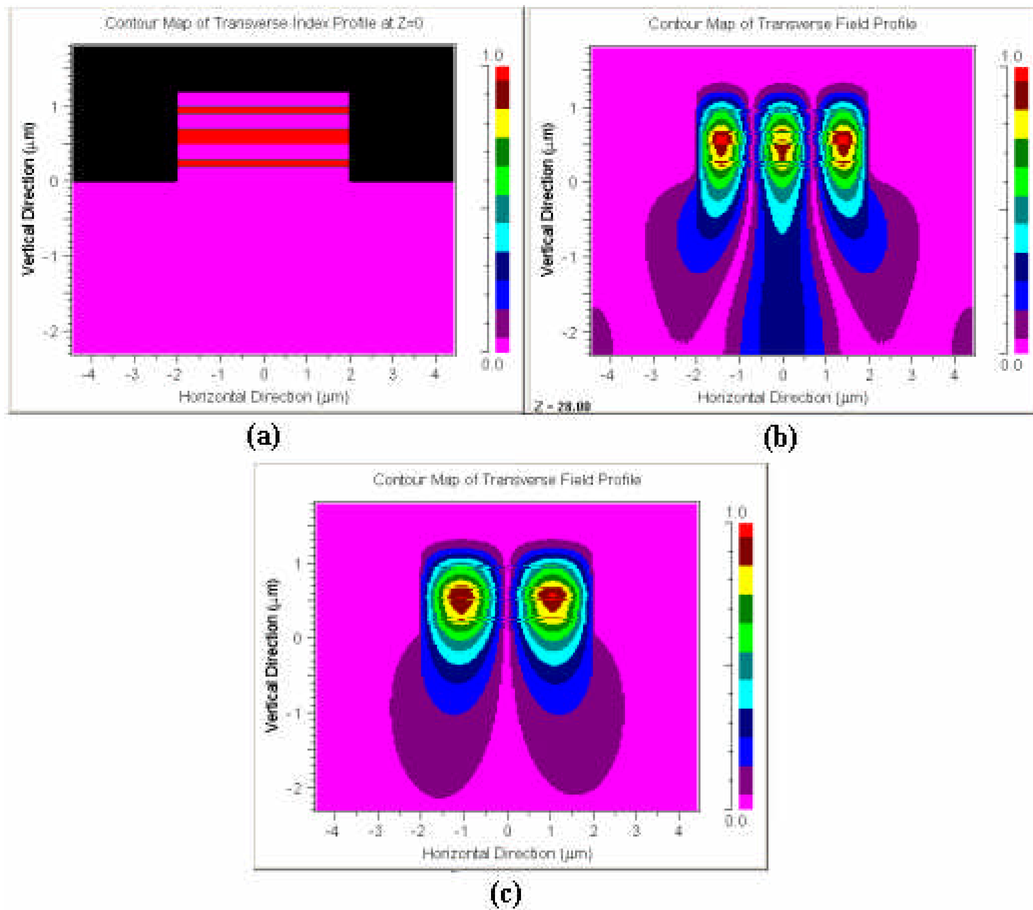


FIGURE 2.14 (a) Waveguide design R998 width = 5µm, (b) associated mode profile (Z=432) and (c) associated mode profile (Z=168)

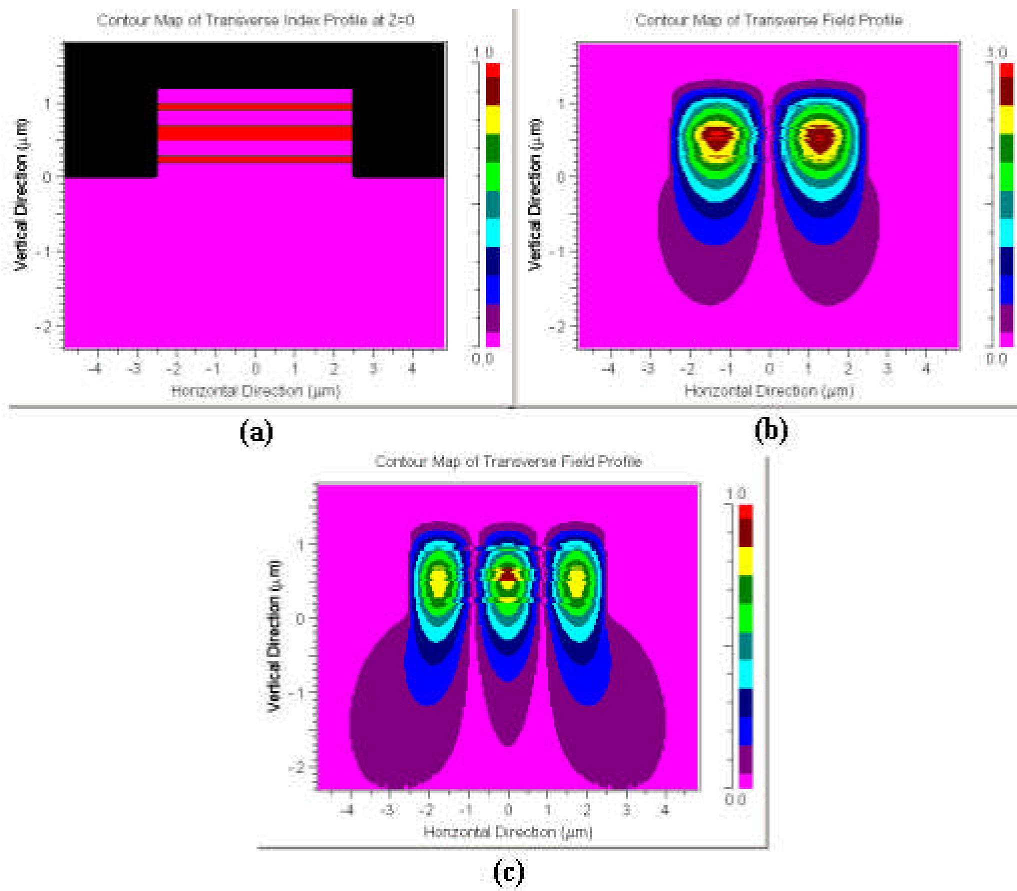


FIGURE 2.15 (a) Waveguide design R998 width = 6μm, (b) associated mode profile (Z=350) and (c) associated mode profile (Z=168)

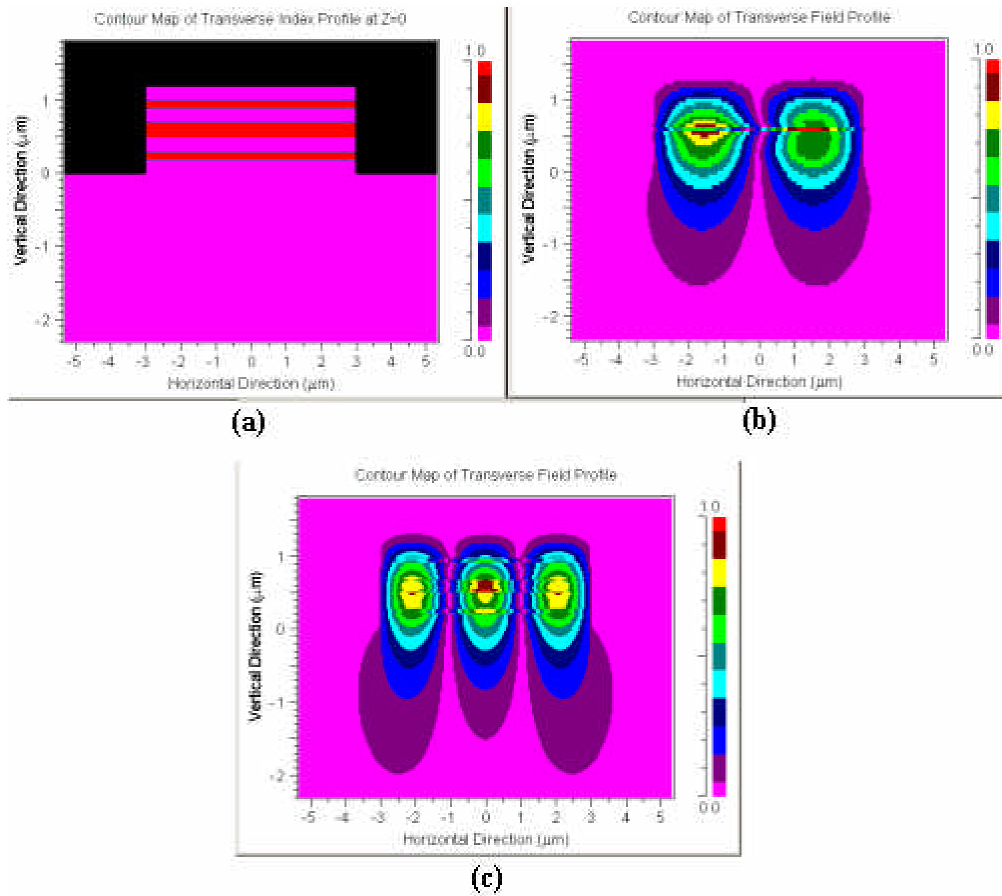


FIGURE 2.16 (a) Waveguide design R998 width = 7µm and (b) associated mode profile (Z=350)

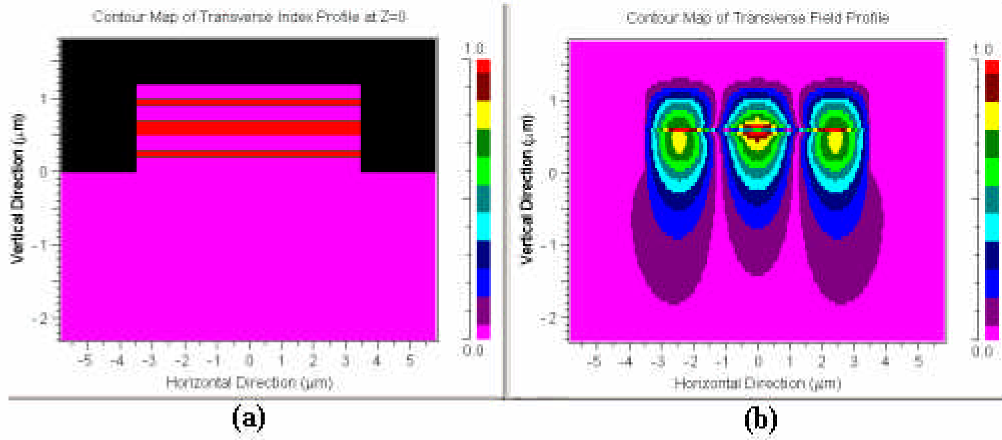


FIGURE 2.17 (a) Waveguide design R1007 width = 1µm and (b) associated mode profile (Z=96)

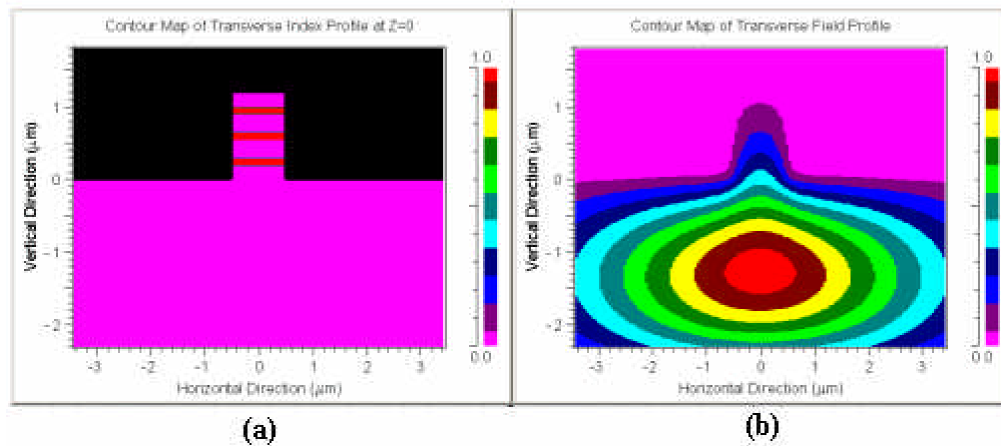


FIGURE 2.18 (a) Waveguide design R1007 width = 2µm and (b) associated mode profile (Z=320)

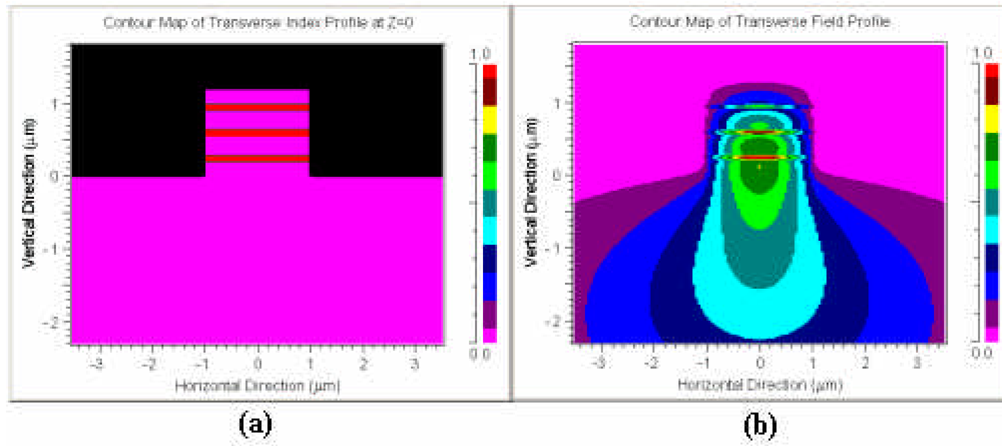


FIGURE 2.19 (a) Waveguide design R1007 width = 3µm and (b) associated mode profile (Z=172)

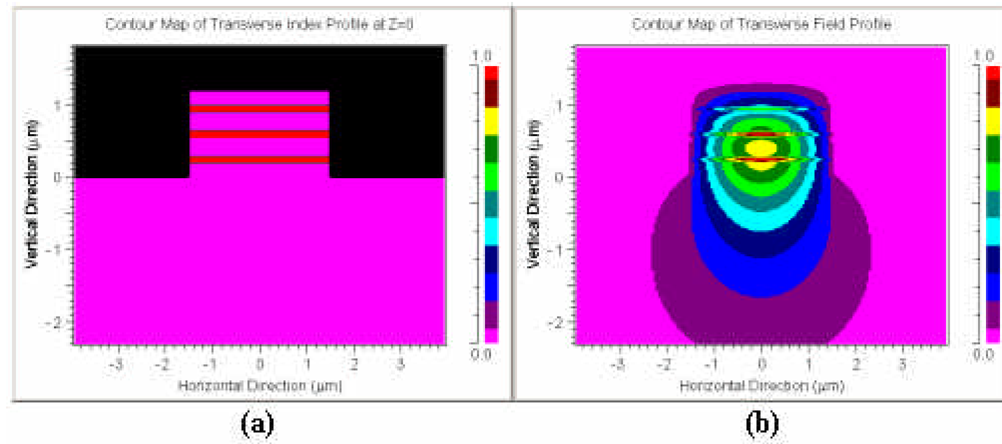


FIGURE 2.20 (a) Waveguide design R1007 width = 4µm and (b) associated mode profile (Z=128)

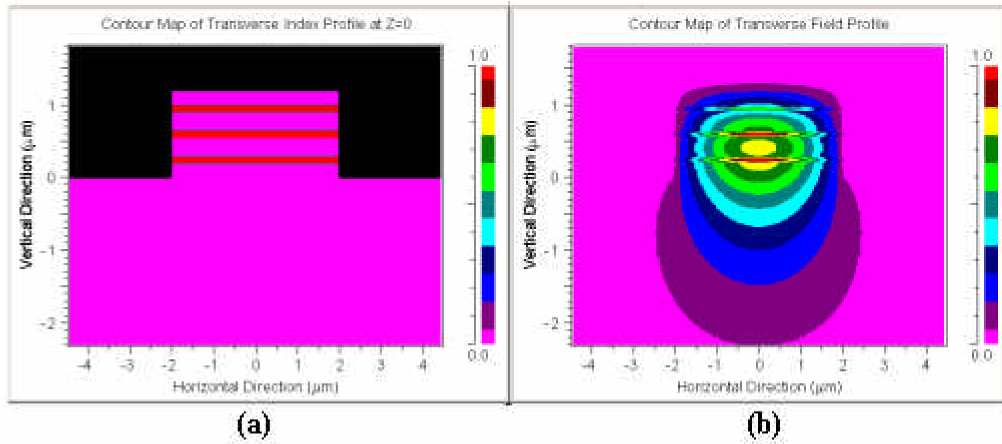


FIGURE 2.21 (a) Waveguide design R1007 width = 5µm and (b) associated mode profile (Z=96)

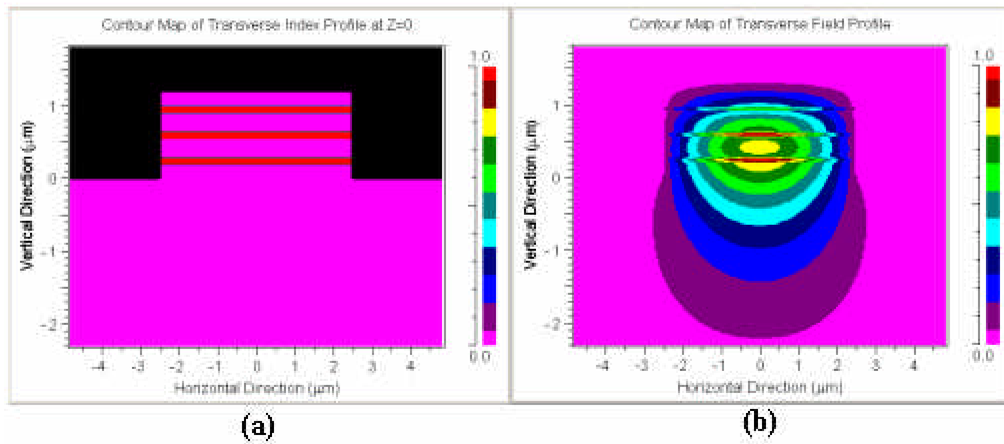


FIGURE 2.22 (a) Waveguide design R1007 width = 6μm, (b) associated mode profile (Z=20) and (c) associated mode profile (Z=196)

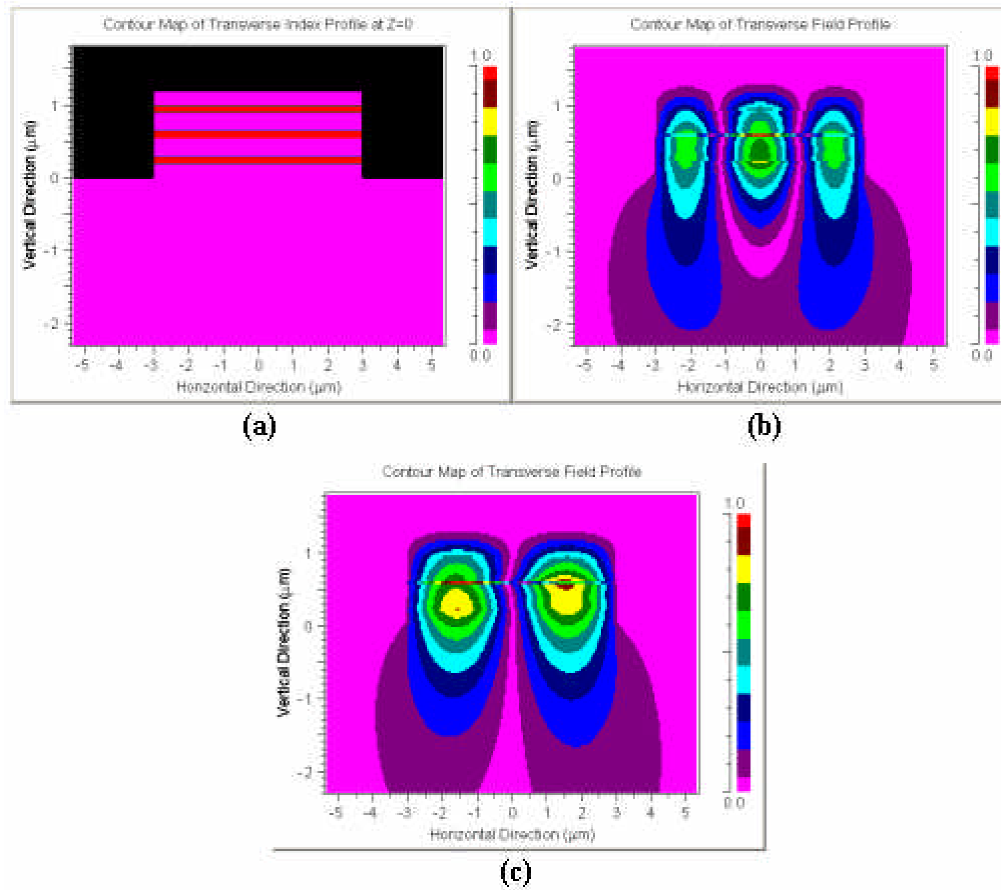
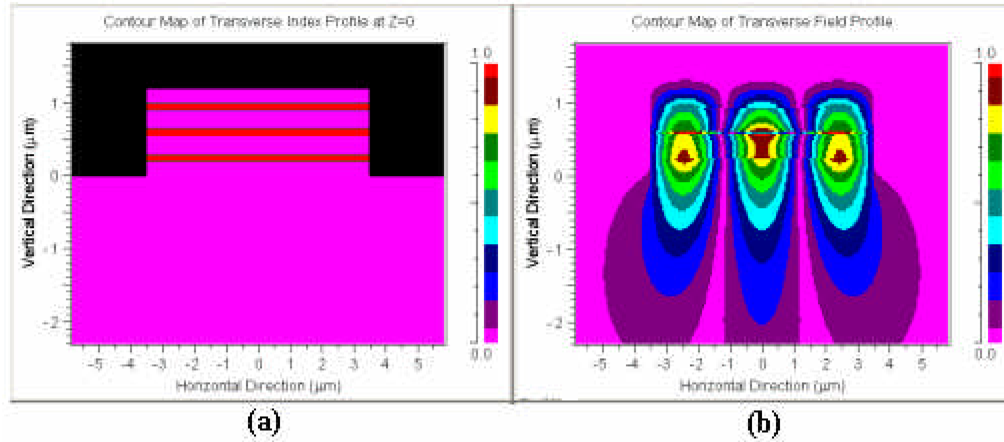


FIGURE 2.23 (a) Waveguide design R1007 width = 7µm and (b) associated mode profile (Z=36)

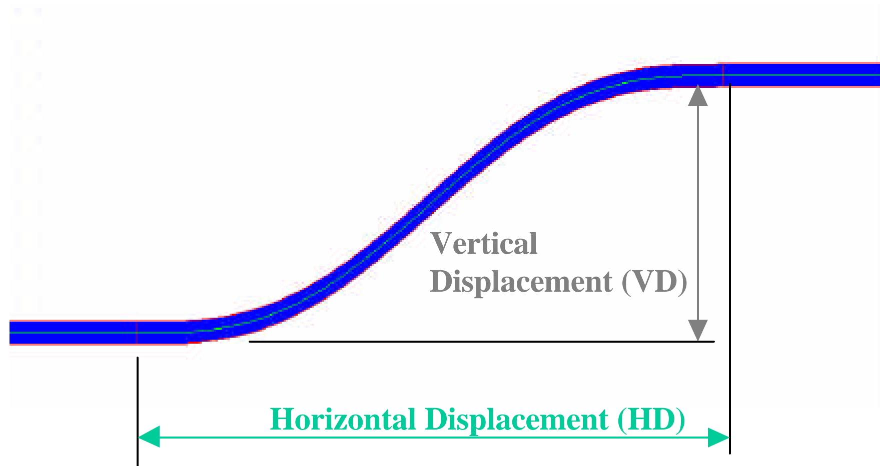


Upon expecation of the simulated results, it is evident that the 1µm waveguide width for both R998 and R1007, are not capable of providing good modal confinement. The mode of the 1µm guides spread and move towards the slab region, resulting in high loss. Both R998 and R1007 seem to be single mode for widths of 2µm and 3µm, with the 3µm guide being less lossy for both cases. It should be noted that the R1007 waveguides seem to contain more loss than the R988 guides of the same width for values of 2µm and 3µm. R998 straight guides of widths 4µm through 7µm all give multimode results. R1007 straight guides of widths 4µm and 5µm are both single mode, their losses seem comparable with those found in the 3µm wide guide. Straight waveguide widths of 6µm and 7µm are both multimode for the R1007 growth. Experimental data will be compared to simulated results.

2.3.2 Mask Design

In order to obtain a substantial range of data for the loss measurements, a number of waveguides have been fabricated varying in width and bending radius. Eight different sine s-bends have been fabricated, with use of an OptiWave waveguide modeling software program, with varying vertical and horizontal displacements, show in Figure 2.24. Radii for the various bends have been determined by mapping a cosine wave with simliar displacement values, to a circle. The horizontal displacements shown are approximately 5% shorter than the displacement values given by the software program, as a result of a small straight waveguide section place and the start and end of each sine s-bend section.

FIGURE 2.24 Example of Sine S-bend showing vertical and horizontal displacements



The displacement and approximate radii values for the sine s-bends are as follows:

sine s-bend (1) VD: 60µm, HD: 190µm, Radius: 179.855µm
sine s-bend (2) VD: 75µm, HD: 150µm, Radius: 142.53µm
sine s-bend (3) VD: 53µm, HD: 115.75µm, Radius: 109.32µm
sine s-bend (4) VD: 167.5µm, HD: 380µm, Radius: 365.59µm
sine s-bend (5) VD: 98µm, HD: 470µm, Radius: 448.66µm
sine s-bend (6) VD: 80µm, HD: 265µm, Radius: 252.14µm
sine s-bend (7) VD: 66.25µm, HD: 132.5µm, Radius: 127.69µm
sine s-bend (8) VD: 385µm, HD: 802.5µm, Radius: 779.46µm

The bends have been separated in two sets. Set A contains s-bends (1) - (4). Set B contains s-bends (5) - (8). X3 is short hand notation representing that there are three identical guides of a particular type. Sets A and B are laid out as follows:

Set A:
Straight waveguide (SWG)
s-bend (1) - four bends separated by straight waveguide sections X3
SWG
s-bend (1) - six bends separated by straight waveguide sections X3
SWG
s-bend (1) - two bends separated by straight waveguide sections X3
SWG
s-bend (2) - six bends superheated by straight waveguide sections X3
SWG
s-bend (2) - four bends separated by straight waveguide sections X3

SWG
s-bend (2) - two bends separated by straight waveguide sections X3
SWG
s-bend (3) - four bends separated by straight waveguide sections X3
SWG
s-bend (3) - six bends separated by straight waveguide sections X3
SWG
s-bend (3) - two bends separated by straight waveguide sections X3
SWG
s-bend (4) - four bends separated by straight waveguide sections X3
SWG
s-bend (4) - two bends separated by straight waveguide sections X3
SWG

Set B:
Straight waveguide (SWG)
s-bend (5) - six bends separated by straight waveguide sections X3
SWG
s-bend (5) - four bends separated by straight waveguide sections X3
SWG
s-bend (5) - two bends separated by straight waveguide sections X3
SWG
s-bend (6) - six bends separated by straight waveguide sections X3
SWG
s-bend (6) - four bends separated by straight waveguide sections X3
SWG
s-bend (6) - two bends separated by straight waveguide sections X3
SWG
s-bend (7) - six bends separated by straight waveguide sections X3
SWG
s-bend (7) - four bends separated by straight waveguide sections X3
SWG
s-bend (7) - two bends separated by straight waveguide sections X3
SWG
s-bend (8) - four bends separated by straight waveguide sections X3
SWG
s-bend (8) - two bends separated by straight waveguide sections X3
SWG

Both sets A and B were fabricated with waveguide widths ranging from 1μm thorough 7μm. A mask was designed containing seventeen six by six millimeter dies, Figure 2.25. All the dies consist of either set A or B, straight waveguides followed by a set of three identical waveguides containing a number of bends; Figure 2.26 depicts an example of a die.

FIGURE 2.25 The mask layout containing the various dies

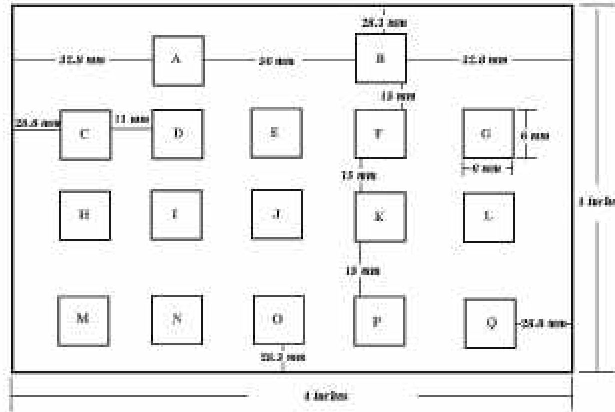
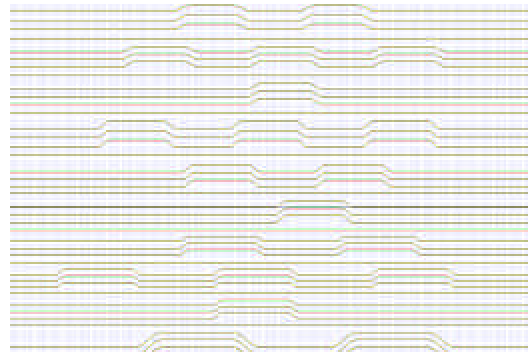


FIGURE 2.26 An example of one of the many dies fabricated, set A



For each bend, there are three duplicates of three identical waveguides. Each duplicate contains a different number of bends. The purpose of this configuration is to ensure the loss measured in the waveguides is linear with the number of bends. Each bend is matched with its mirror image (y-axis), this is to insure that the entry and the exit points lay on the same line, for ease in measuring. Dies C thorough I contain set A with widths 1 thorough 7μm respectively and dies J thorough P contain set B with widths 1 thorough 7μm respectively. Die A contains waveguide bends (1) thorough (4) with offsets of 0.2, 0.4 and 0.6μm. Die B contains waveguide bends (5) thorough (8) with offsets of 0.4, 0.4 and 0.6μm. Figure 2.27 depicts an example of an offset guide. As before, for die A and B, each bend is fabricated in a duplicate of three per offset, each set is followed by a straight waveguide. Die Q contains a set of total internal reflection bends. Figure 2.28

depicts the three different total internal reflection bends with their dimensions. The total internal reflection bends were designed in duplicates of three, various sets contained a different number of bends. Each set was separated by a straight waveguide.

FIGURE 2.27 Example of a waveguide offset between the bent and straight sections of the guide

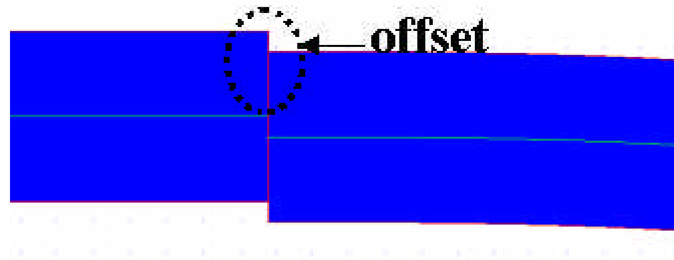
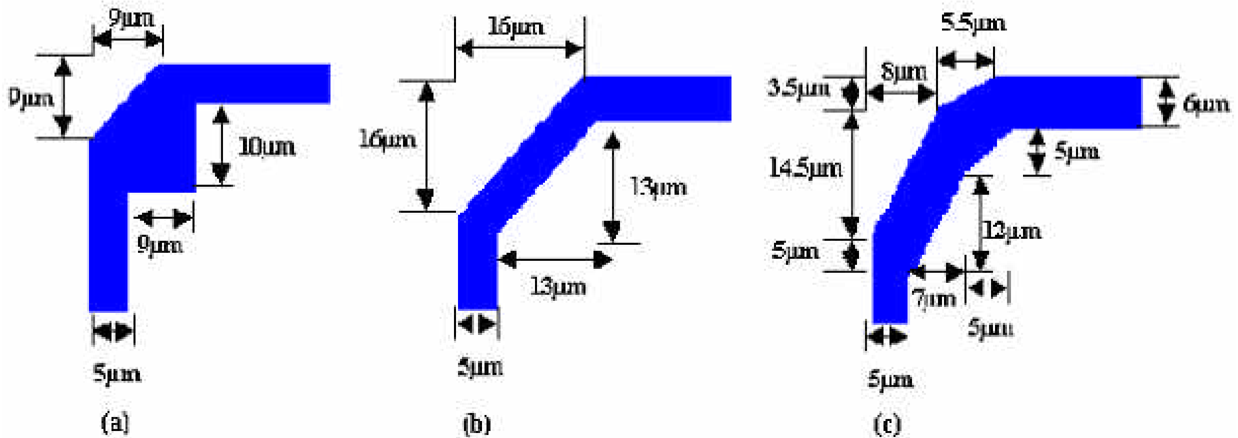


FIGURE 2.28 Total internal reflection bends. (a) Resonator bend. (b) Corner mirror bend. (c) Double corner mirror bend



3.0 RESEARCH APPROACH

3.1 Research Objective

The goal is to design and fabricate low loss passive InP waveguide bends. A variety of bending radii and waveguide widths will be tested and measured for loss. The dimensions of an ideal low loss bend are to be found for future use in photonic integrated circuits.

The waveguides will be fabricated in a InGaAsP material system. The dimensions of the waveguide, height and width, will greatly effect the mode profile and the loss in the waveguide. All of the waveguides will have a total height of 1.2µm while the width varies from 1 µm to 7µm. Two different structures were grown and will be investigated, R998 and R1007. The waveguides will contain an even number of bends so the entry and exit point of the guide lies on the same plane, for ease of measuring.

3.2 Fabrication Sequence

The follow fabrication sequence contains the steps which were taken to fabricate the passive waveguide bends.

FIGURE 3.29 Molecular epitaxy growth R998 (a) and R1007 (b)

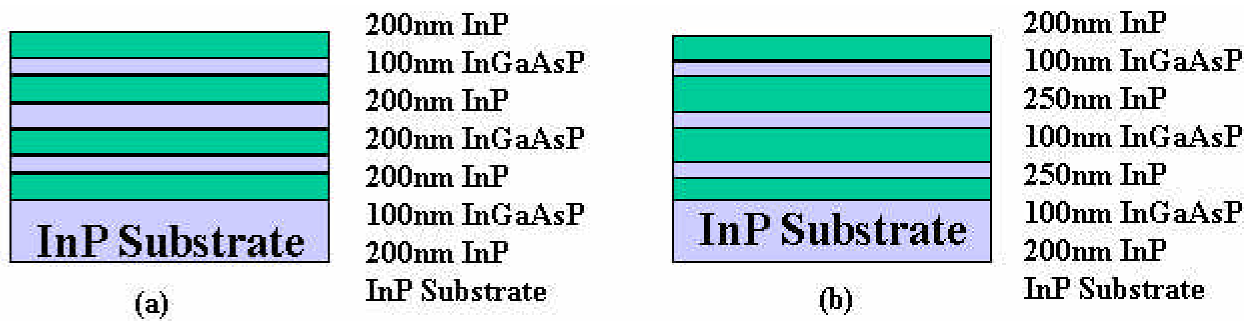
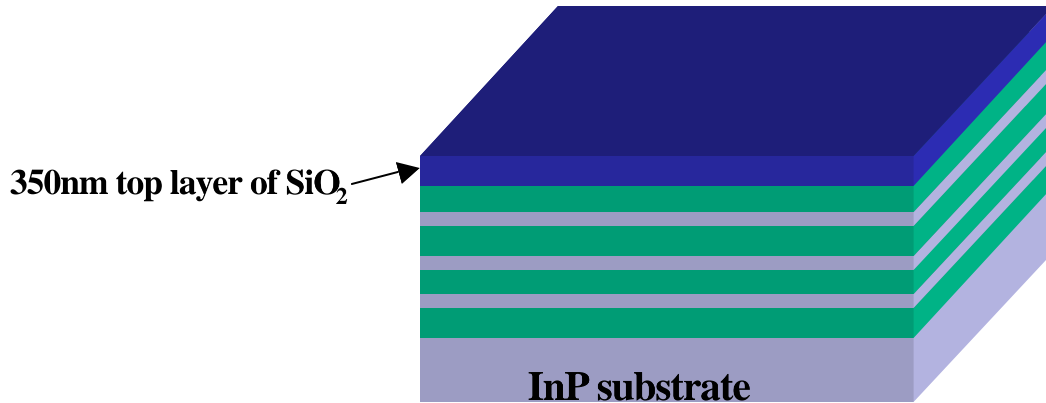


Figure 3.29 shows two grown structures as a result of Molecular beam epitaxy (MBE). After the InP wafer contains the grown films on its substrate, the wafer was cleaved into quarters. Figure 3.30 depicts the next step in the process.

FIGURE 3.30 Top layer of SiO_2 deposited on growth



A 350nm layer of SiO_2 was deposited with use of a sputter system in the Nanostructures Laboratory (NSL). SiO_2 is used as a hard mask during the etch of the MBE grown structure.

FIGURE 3.31 Photolithography process

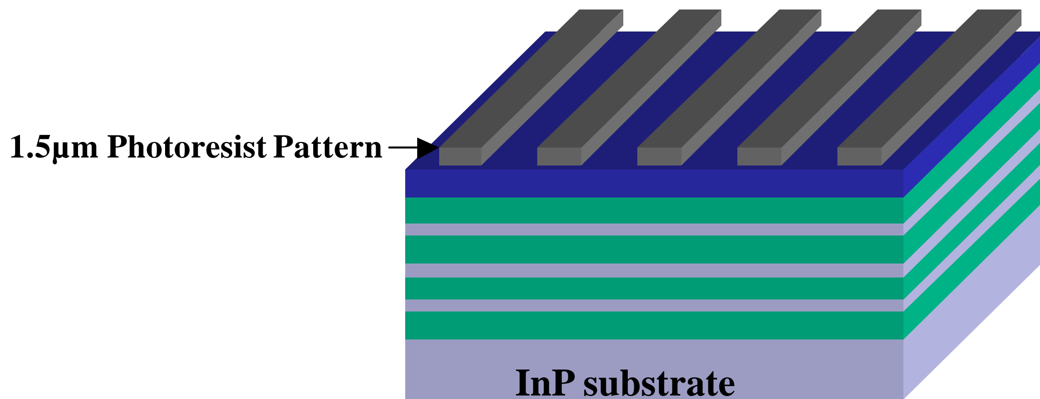
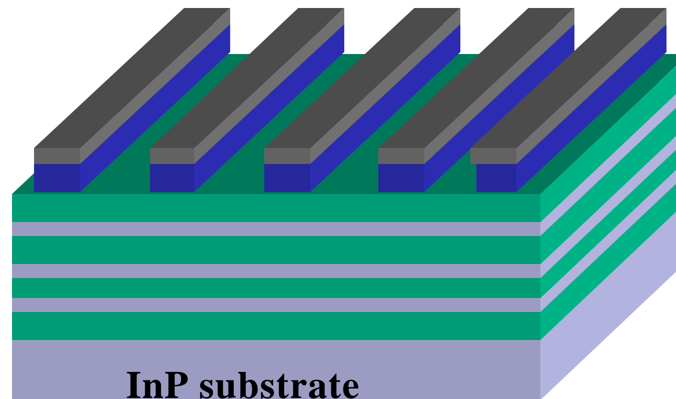


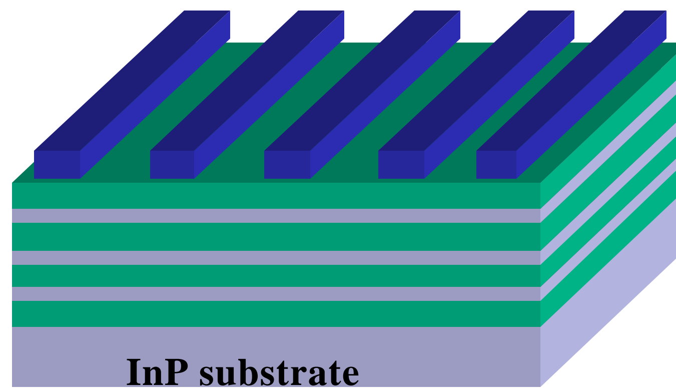
Figure 3.31 shows the results of the photolithography process, also done in NSL as were all the remaining processing steps. The photolithography process is necessary in order to pattern the SiO_2 hard mask. The photoresist pattern was used as a mask for etching SiO_2.

Figure 3.32 (a) depicts the results of the SiO_2 etch where the photoresist pattern was used as a mask, notice the same patterns which were formed on the photoresist have been transformed to the SiO_2 layer.

FIGURE 3.32 Results after SiO_2 (a) and Ash (b)



(a)



(b)

Figure 3.32 (b) depicts a sample after an ashing step where the photoresist has been stripped away. The SiO_2 pattern is now used as a hard mask for etching in to the InP/InGaAsP layers.

FIGURE 3.33 Results after RIE etching

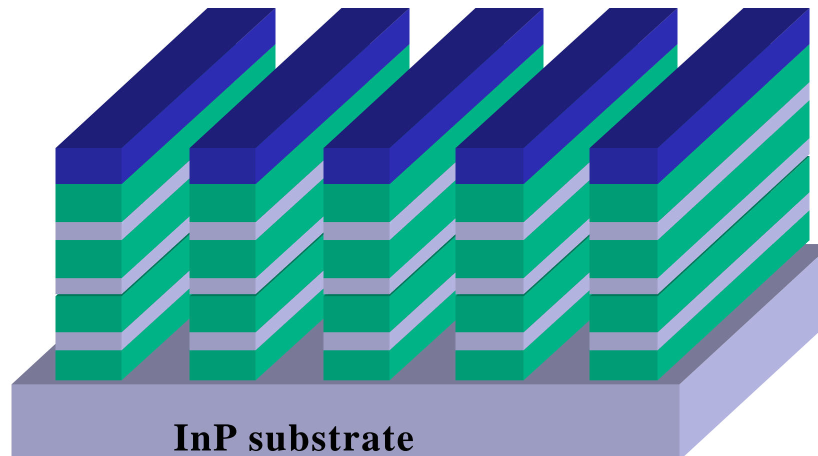


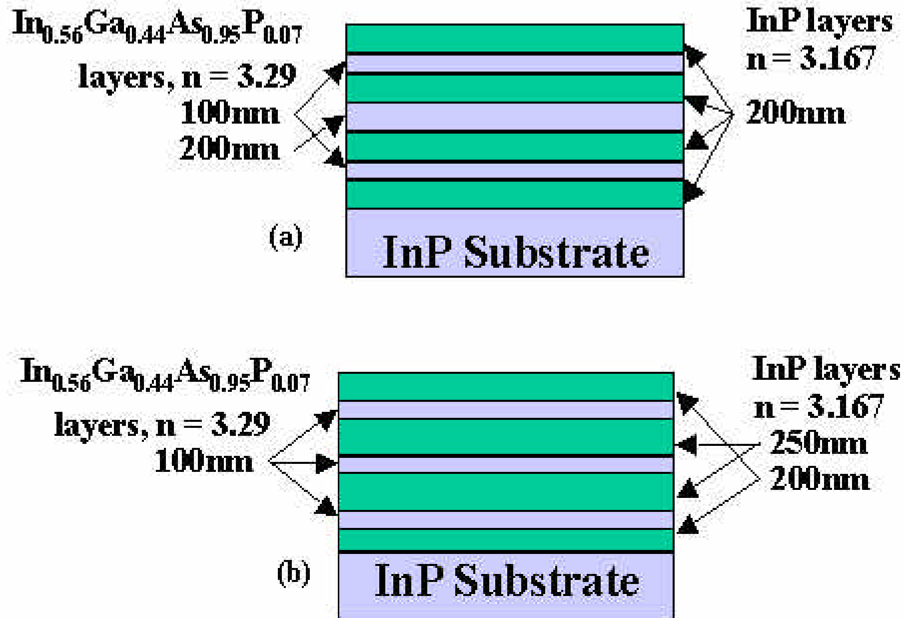
Figure 3.33 shows the final step of the process, where the SiO_2 pattern is used as a hard mask for reactive ion etching (RIE). RIE etches down to the InP/InGaAsP layers stopping at the substrate, for a total of 1.2µm. Since the actually devices will have a top layer of SiO_2, a final SiO_2 etch is omitted.

4.0 FABRICATION DISCUSSION & RESULTS

4.1 Molecular Beam Epitaxy Results

Two structures, R998 and R1007, were grown using the Riber Instruments gas source molecular beam epitaxy system. Molecular beam epitaxy is a thin film technique capable of controlling layer thickness and composition precisely and of growing uniform ultra thin layers with abrupt interfaces [9]. Figure 4.34 displays the dimensions of the grown structures.

FIGURE 4.34 MBE grown structures R998 (a) and R1007 (b)

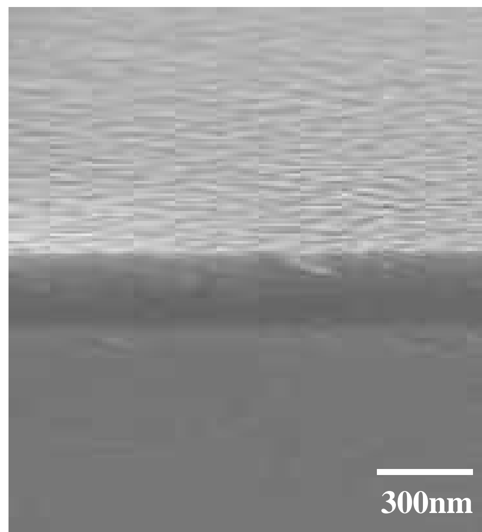


The quarternary $In_{0.56}Ga_{0.44}As_{0.95}P_{0.07}$ layers were used for the purpose of raising the effective index of the guiding layer, so that the guiding layer contains an effective index higher than the InP substrate and the top cladding layer. The growth process was performed on whole wafers, which were later cleaved to quarter wafers for further fabrication.

4.2 Photolithography Results

Photolithography is used to transfer the waveguide images via a photo-mask, Figure 2.25 and Figure 2.26, to the substrate. The first step in the photolithography process is to deposit approximately 350nm of SiO_2 on quarter wafer samples, using a sputtering system. Figure 4.35 depicts the results of a sample having undergone the SiO_2 deposition process. SiO_2 is used as a hard mask in plasma etches which take place later on in the process flow.

FIGURE 4.35 SEM of 350nm thick SiO_2 layer used as a hard mask in future fabrication steps



Following the SiO_2 deposition, HMDS and photoresist is spun on the sample and then baked. HMDS, or Hexa Methyl Di Silazane, is typically used in the semiconductor industry, to improve the adhesion of photoresist to oxides by reacting with both the oxide and resist surfaces. The HMDS was applied to the wafer, left to sit for 30 seconds and then spun for 1 minute at 3000rpm. The photo-mask was designed for the use of a positive photoresist, therefore an approximately 1.5 µm layer of 1813 resist was spun on the sample at 3000rpm for 1 minute, followed by a 30 minute bake in an oven with a temperature of 90°C. Contact exposure was performed using a Tamarack UV exposure system. Shipley 352 developer was used in the final development stage of the photolithography process.

4.2.1 Photolithography Problems & Solutions

Initially, the quarter wafer sample were first cleaved into five 7mm square samples prior to spinning the resist. This caused a build up of resist on the edge of each sample. Acetone was used as a failed attempt at removing this edge bead. Because of the resist edge bead, complete contact could not be made between the photo-mask and sample. The appearance of Newton rings resulted from the poor contact and allowed the transfer of undesired patterns unto the sample. Figure 4.36 is a SEM image showing the formed patterns. A trench along the sidewall of the waveguides also resulted, depicted in Figure 4.37. Spinning and baking the resist on the quarter wafer sample before cleaving the sample, resulted in better contact and eliminated the Newton rings. Two scrap SiO_2 half wafer pieces were placed to the left and right of the sample to improve the leveling of the photo-mask over the sample.

FIGURE 4.36 Pattern due to poor contact during UV exposure

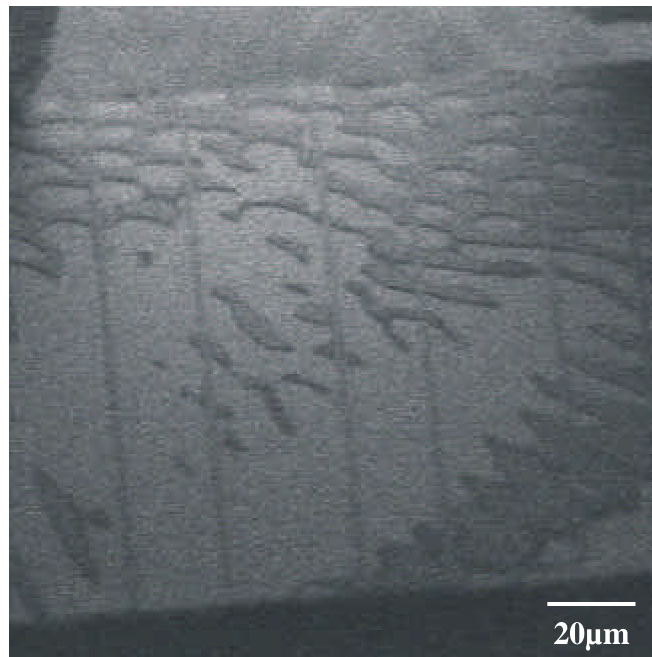
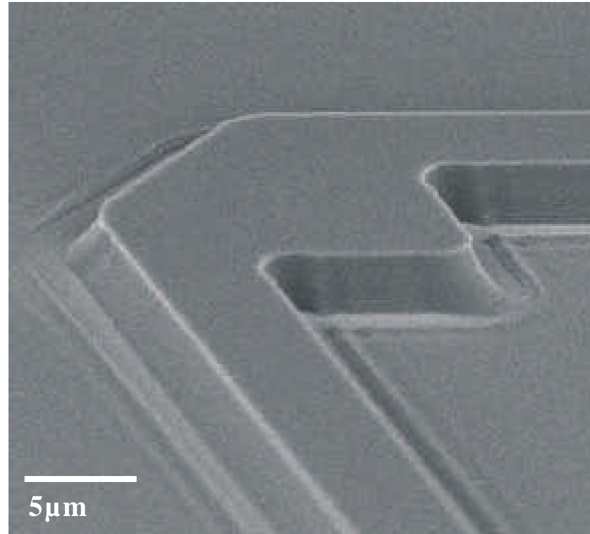


FIGURE 4.37 Sidewall trench due to poor contact during UV exposure



It was discovered that the exposure and development time greatly effected the side profile of the waveguide. Over exposure led to the rounding of waveguide sidewalls, (Figure 4.38), while over development will lead to undercutting, (Figure 4.39). An optimal exposure and development time was determined as 10 seconds and 1 minute and 30 seconds respectively. The optimal time did not contain sidewall rounding and a greatly reduced undercut, Figure 4.40.

FIGURE 4.38 Over exposed sample. 30 second exposure and 1minute development time

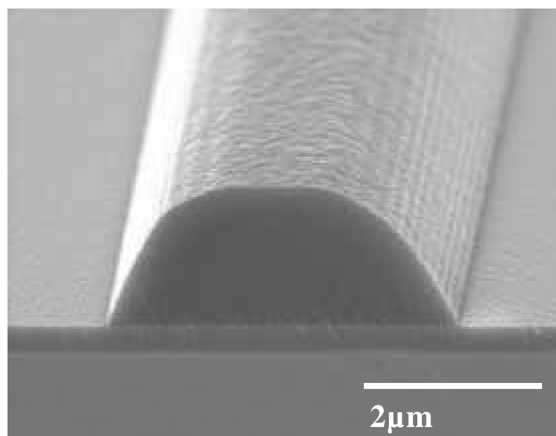


FIGURE 4.39 Over developed sample.10 second exposure and 2 minute development time

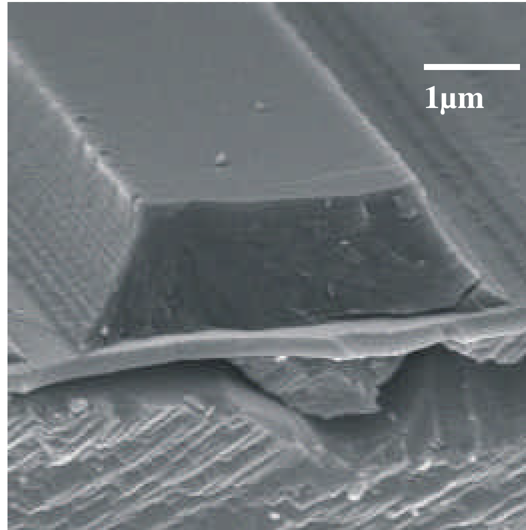
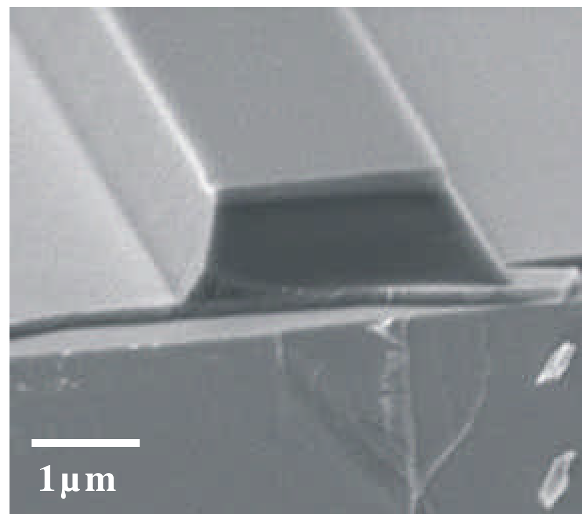


FIGURE 4.40 Optimum exposure and development times of 10 seconds and 1 minute and 30 seconds respectively



4.3 Reactive Ion Etching Results

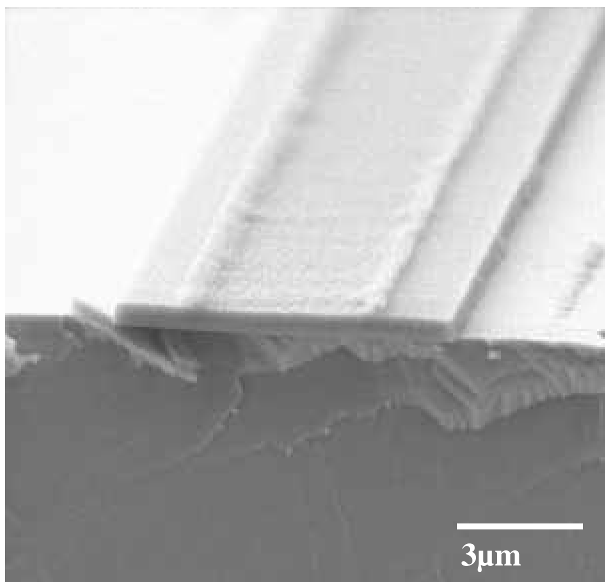
Reactive ion etching (RIE) is a plasma-based etching technique where the material, which is etched, is removed as a volatile gaseous species [10]. Etching occurs by a chemical reaction between the material to be etched and the atoms produced in the plasma. While choosing an etch mask, careful consideration on etching compatibility must be taken into account. With the use of an etch mask, reactive ion etching transfers the exposed pattern to the epilayers.

4.3.1 SiO_2 Reactive Ion Etch

The first step following the photolithography process is a CHF_3 plasma etch, using a PlasmaTherm RIE etcher, where the photoresist is used as the SiO_2 etch mask. CHF_3 will not etch through the resist mask, making it a suitable choice for the etch but there are difficulties with long etch runs. This specific etch, when run for long periods of time, results in polymer deposition on the chamber walls. Therefore a CF_4 and O_2 clean run as well as wiping the chamber with methanol, must be performed prior to and after each etch run. The CF_4 and O_2 clean run was performed for 15 minutes with the following parameters: 300W, 25mT and 350V. The CHF_3 plasma etch was performed for 15 minutes and 40 seconds three samples at a time. The parameters for the CHF_3 plasma etch were as follows: 300W, 10mT and 300V.

After successfully etching the SiO_2 layer using the photoresist as a mask, the pattern produced by photolithography has now been transferred to the SiO_2 layer. The next step in the process is to remove the top layer of photoresist with the use of an asher, a low powered O_2 RIE. To reduced the amount of time necessary for the ashing run, the sample is rinsed with acetone. Ashing was done with a pressure of 3.5mT for 5 minutes, three samples at a time. Figure 4.41 depicts a sample having undergone a RIE etch of SiO_2 and ash step. Notice on Figure 4.41 that there is still a small amount of residual photoresist left on top of the waveguide, this particular sample had not undergone a acetone rinse prior to ashing. The left over resist does not have an effect on later processing steps.

FIGURE 4.41 Results after RIE etch of SiO_2, using photoresist as a mask, and ashing. SiO_2 pattern above the epilayers is all that remains after the process



4.3.2 InP/InGaAsP Reactive Ion Etch

Once the waveguide patterns have been transferred to the SiO_2 layer, the sample is ready for a RIE etch of the InP/InGaAsP layers. Prior to etching the epilayers, a clean is first performed in the chamber. The clean was performed with O_2 and CF_4 with flow rates of 29.2 and 28.2 sccm respectively. The InP/InGaAsP runs were performed with CH_4 and H_2 with flow rates of 10 and 20 sccm respectively. The RF power that used for the run was approximately 100W and a DC bias of approximately 120V, produced an etch rate of 31nm/min. Due to a polymer by product of the CH_4 / H_2 etches, a cleaning run must be performed after every InP etching run. Since the final optical logic device will have a top layer of SiO_2, the SiO_2 hard mask is not removed.

4.3.3 InP/InGaAsP Reactive Ion Etching Problems & Solutions

Initial test runs were performed on blank InP samples. Desired results were achieved with CH_4 / H_2 flow rates of 10/20 sccm, pressure of 10mT and a RF power of 50W yielding an etch rate of 1µm/min, Figure 4.42. It was discovered that etching rates change when the same parameters were used with the InP/ InGaAsP structure. The first quaternary layer actual acted as an etch stop regard-

less of the etch duration, Figure 4.43. Decreasing the RF power to 150W and decreasing the pressure to 4mT, resulted in etching both the quaternary layers as well as the InP. The use of 150W of RF also disintegrated the SiO_2 etch mask causing sputtered SiO_2 to be deposited on the substrate, Figure 4.43. A final optimization was made by reducing the RF power to 100W, Figure 4.45. Notice in Figure 4.45 the SiO_2 etch mask remains intact and there is an improvement in the sidewall smoothness. Also, upon careful expectation of Figure 4.45, the individual quaternary layers of the grown structures may been seen.

FIGURE 4.42 Initial RIE results performed on InP samples, RF power = 50W pressure = 10mT

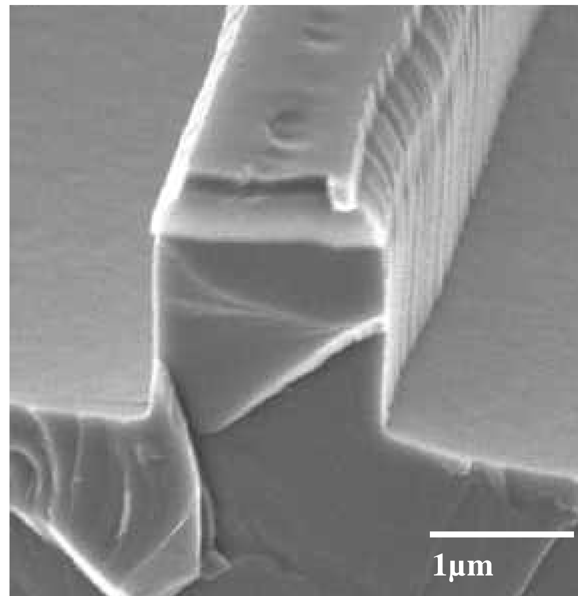


FIGURE 4.43 Initial RIE results performed on the InP/InGaAsP grown structure, RF power = 50W pressure = 10mT

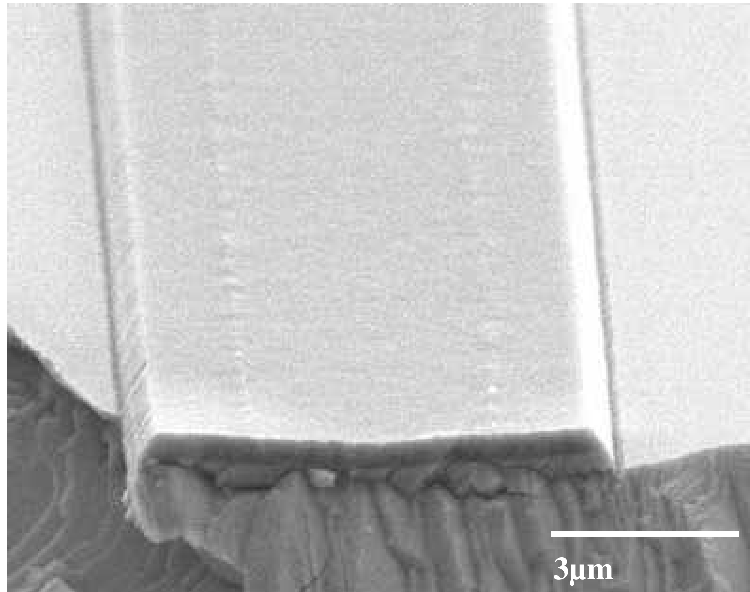


FIGURE 4.44 RIE results on the grown InP/InGaAsP substrate, RF power = 150W pressure = 4mT

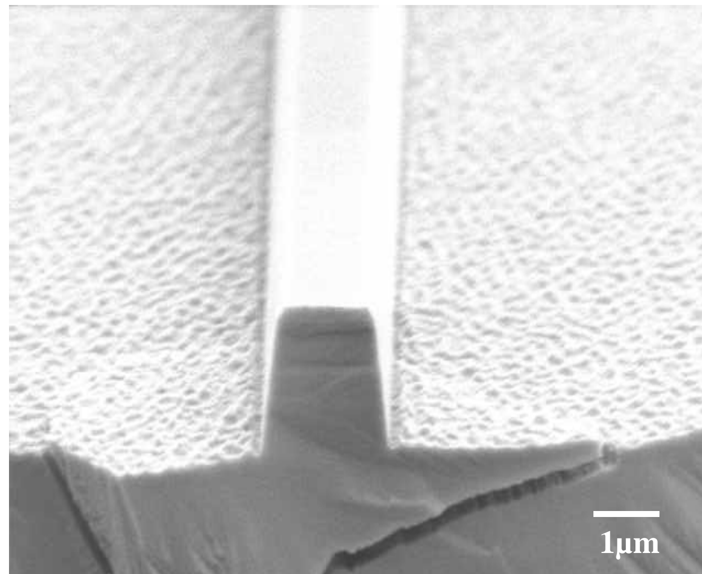
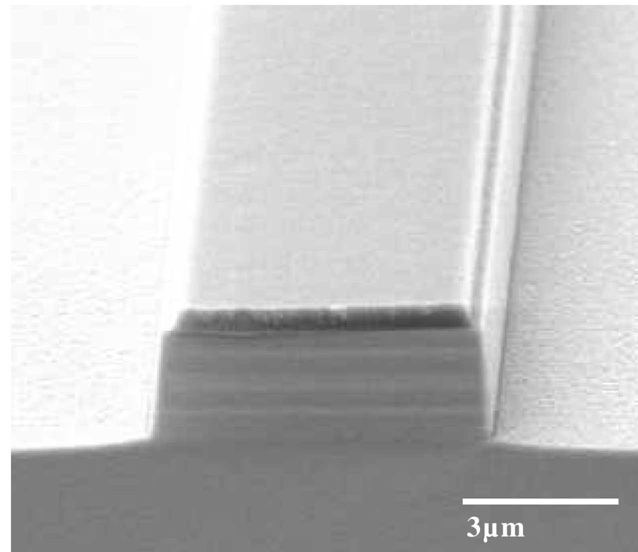
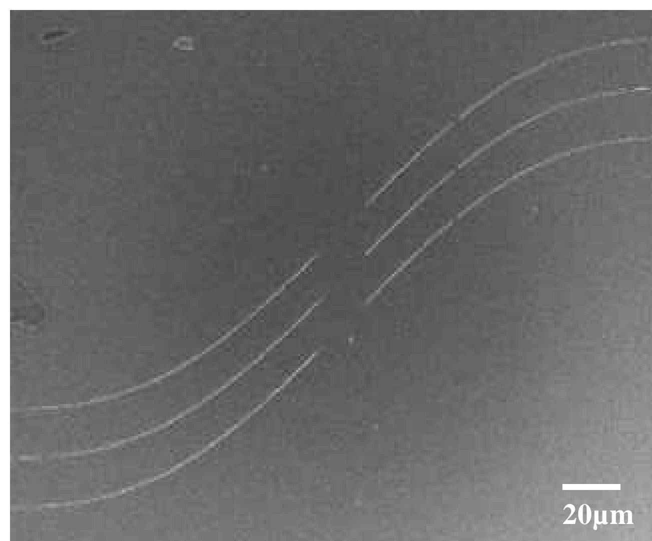


FIGURE 4.45 RIE results on the grown InP/InGaAsP substrate, RF power = 100W pressure = 4mT



Problems were also found with the Reactive Ion Etching of 1µm waveguides. Many of the 1µm waveguides contained breaks after the InP/InGaAsP RIE process, Figure 4.46.

FIGURE 4.46 1µm waveguide breaks due to the InP/InGaAsP RIE process



4.4 Images of Fabricated Waveguides

The following figures are SEM images of a few of the designed waveguide bends, which have gone through the entire fabrication process. Figure 4.47 and Figure 4.48 are examples of total internal reflections bends. Figure 4.49 depicts a set of offset bends, while Figure 4.50 shows a close-up view of one of the offsets. Figure 4.51 portrays a group of sine s-bends.

FIGURE 4.47 Total Internal Reflection Bend, Resonator Bend

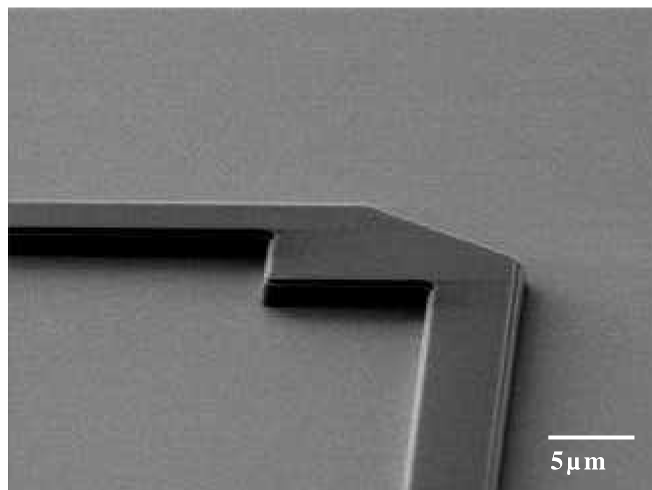


FIGURE 4.48 Total Internal Reflection Bend, Corner Mirror Bend

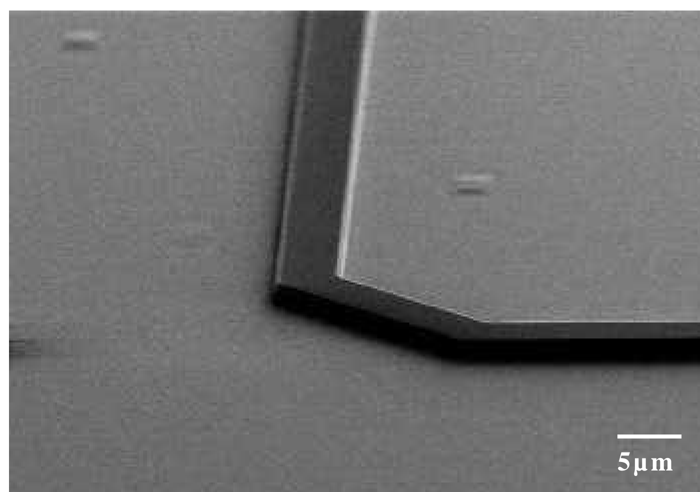


FIGURE 4.49 A group of offset waveguide bends

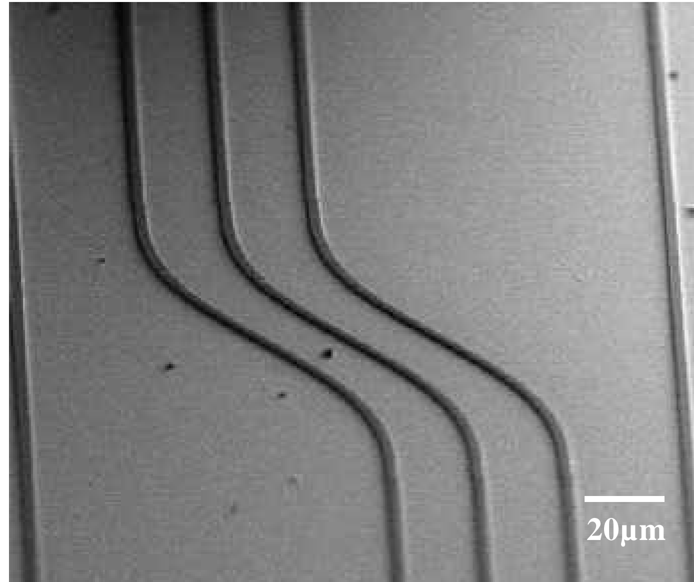


FIGURE 4.50 00000000000000Close up of an offset

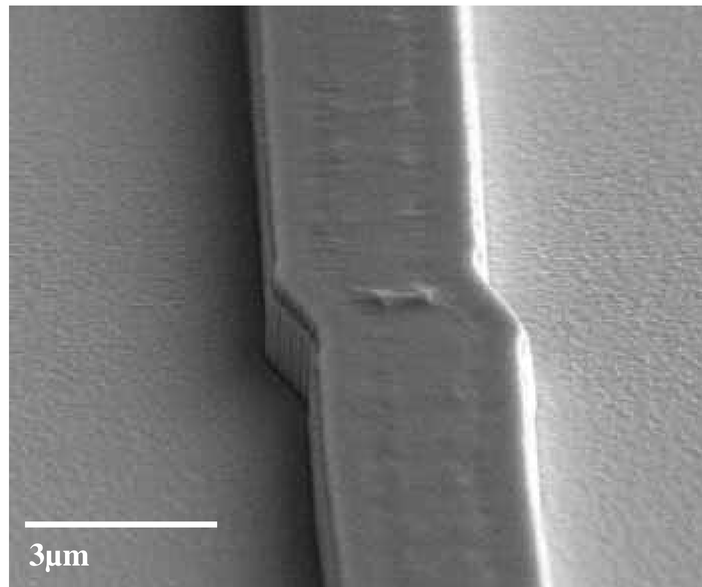
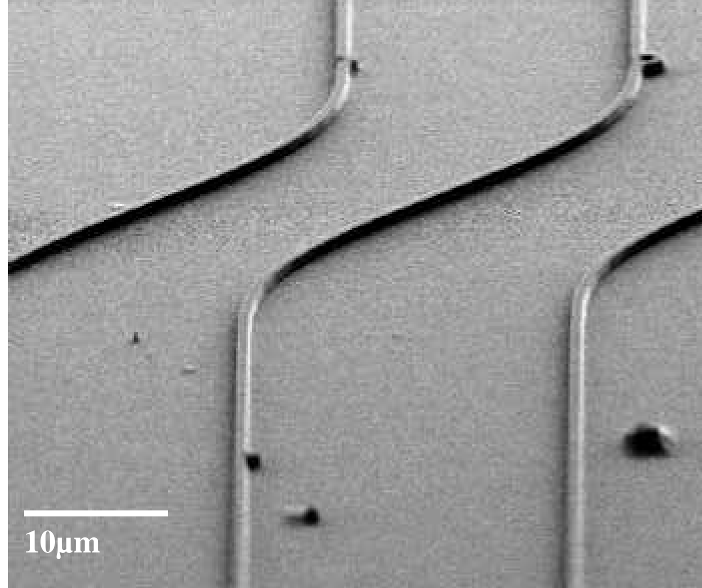


FIGURE 4.51 A group of sine s-bends



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